AMENDMENT TO THE SPECIFICATION

IN THE SPECIFICATION:

A marked up copy of the changes to selected paragraphs are provided below. Please enter these changes to the specification in the record.

Please replace paragraph [0038] with the following amended paragraph:

[0038] A third resistor 60 and a first capacitor 58 connected in series with one another form a RC network 64. The RC network 64 is connected to the source of the first nFET 32 and the ground rail 28. Also connected between the source of the first nFET 32 and the ground rail 28 is a pFET 54 and a third nFET 56. The pFET 54 and the third nFET 56 are connected in series with one another with the drain of the pFET 54 and the drain of the third nFET 54 connected to one another. Additionally, the drain of the first pFET 54 and the drain of the third nFET 56 are connected to the gate of the second nFET 30. The gate of the pFET 54 and the third nFET 56 are connected to the output of the third resistor 60 and the input of the first ~~resistor~~ capacitor 58.

Please replace paragraph [0054] with the following amended paragraph:

[0054] For example, during an ESD event, the voltage on the power supply (Curve #[[1]] 5) rises to a predetermined value of about 1.95V while the voltage at the gate of the first nFET (Curve #[[2]] 6) rises to about 1.3V before the power clamp is switched into the on-state during an ESD event. The voltage across the first and second nFETs (Curve #[[3]] 7) rises to about 1.0V and the voltage at the second nFET (Curve #[[4]] 8) rises to about 0.75V before the power clamp shunts the ESD event to the ground rail. As Figure 6 shows, all values immediately drop when the power clamp is triggered.